

MEMORY TEST DISK INSTRUCTIONS

The memory test disk will test all of the Dynamic RAM and report the first failure that occurs. It reports the failing address, the bad data it read and the data it expected. This makes it easy to find and fix memory IC failures. To run the test, insert the disk in the top drive and apply power. The test will start by itself and give the following information on the display:

Memory Test in
Progress: Sgmt=1

As the test progresses the segment number will be updated to reflect the current segment under test. When a failure occurs, the display will change to inform you the address of the failure, the bad data and the data it expected. Below is an example failure that would be displayed if address 40910 had failed:

Error At 40910
Data: DE S/B: DF

NOTE: Data is what was read back. S/B is what the data should be.

Using the memory layout (see memory theory of op) we can determine which row the bad IC is in. Address 40910 corresponds to Memory board IC 2-9. This is the piggyback board that sits on top of the digital board. Now that the bad row has been isolated the IC can be found. This is done by determining which bit is bad using the information on the display. We must first convert the good and bad data to binary then compare them as shown below:

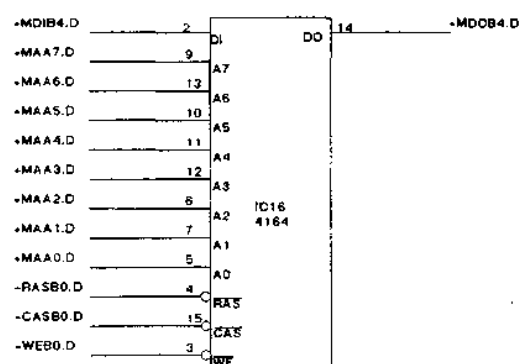
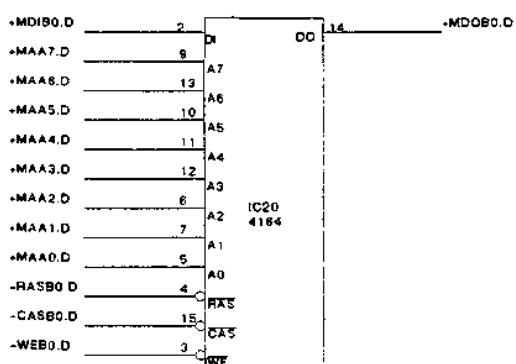
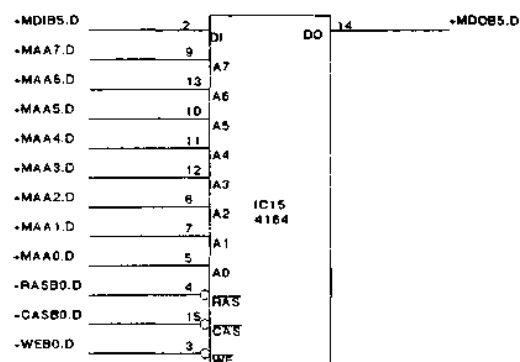
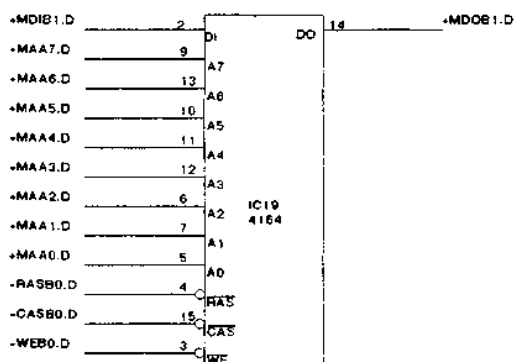
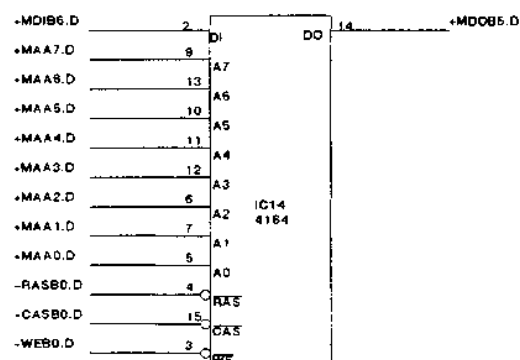
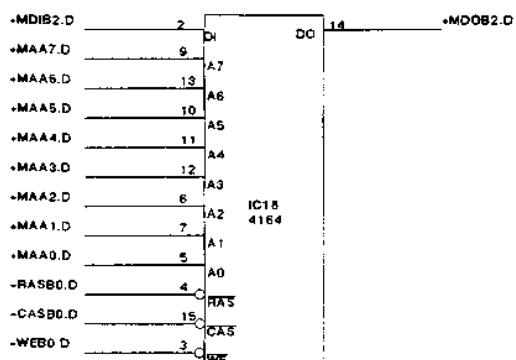
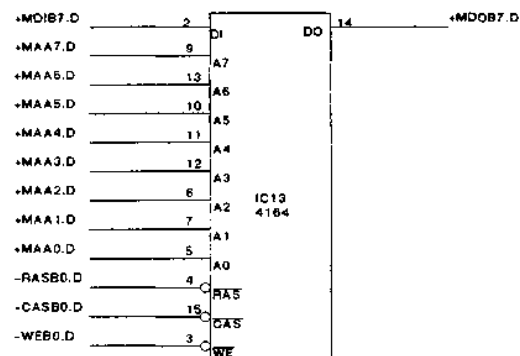
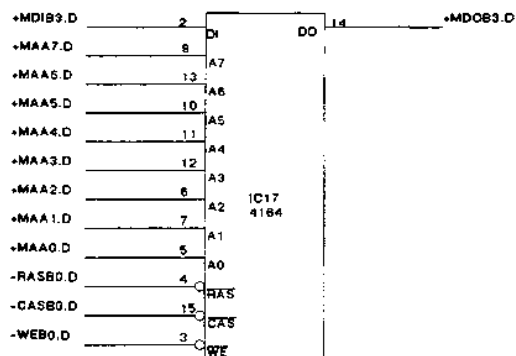
Data DE = 11011110
S/B DF = 11011111

This shows us that data bit 0 is 0 when it should be 1. We can now use the schematic to find which IC is bit 0. Refer to page 3 of 6 for the memory option board and we see that IC 2 thru 9 are on this page. To find bit 0 look at pin 14 of each IC until the signal name for bit 0 (MDOBO.D) is found, which is IC 9. Replace IC 9 to fix the problem.

NOTE: MDOBO.D stands for Memory Data Output Bit 0 . Digital.

EMULATOR 2 MEMORY ORGANIZATION

Memory Address	Segment #	Memory	Location
7FFF--			
----->	F (15)	top segment of DRAM	Mem Bd IC 29-36
78000--			
77FFF--			
----->	E (14)		Mem Bd IC 29-36
70000--			
6FFFF--			
----->	D (13)		Mem Bd IC 20-27
68000--			
67FFF--			
----->	C (12)		Mem Bd IC 20-27
60000--			
5FFFF--			
----->	B (11)		Mem Bd IC 11-18
58000--			
57FFF--			
----->	A (10)		Mem Bd IC 11-18
50000--			
4FFFF--			
----->	9 (9)		Mem Bd IC 2-9
48000--			
47FFF--			
----->	8 (8)		Mem Bd IC 2-9
40000--			
3FFFF--			
----->	7 (7)		Dig Bd IC 71-78
38000--			
37FFF--			
----->	6 (6)		Dig Bd IC 71-78
30000--			
2FFFF--			
----->	5 (5)		Dig Bd IC 51-58
28000--			
27FFF--			
----->	4 (4)		Dig Bd IC 51-58
20000--			
1FFFF--			
----->	3 (3)		Dig Bd IC 32-39
18000--			
17FFF--			
----->	2 (2)		Dig Bd IC 32-39
10000--			
0FFFF--			
----->	1 (1)		Dig Bd IC 13-20
08000--			
07FFF--			
	0 (0)	Low segment of DRAM	Dig Bd IC 13-20
02800			
027FF			
----->	0 (0)	Static RAM	Dig Bd IC 59
02000			
01FFF			
00000	0 (0)	EPROM	Dig Bd IC 42
00000--			

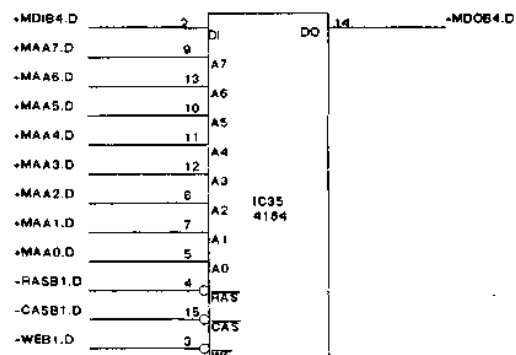
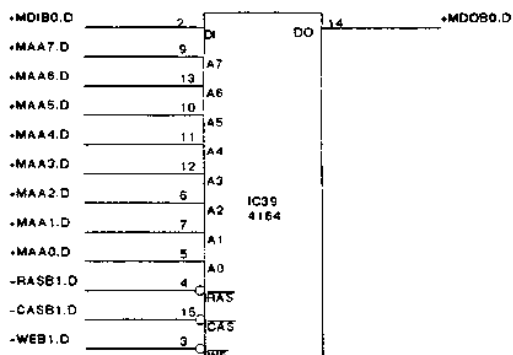
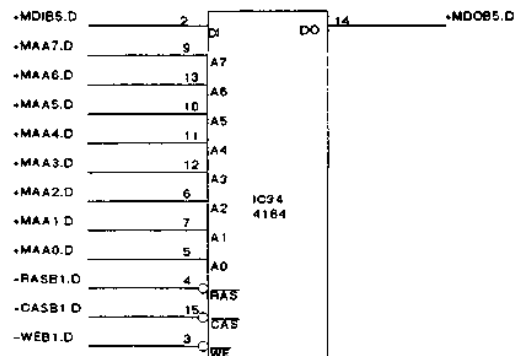
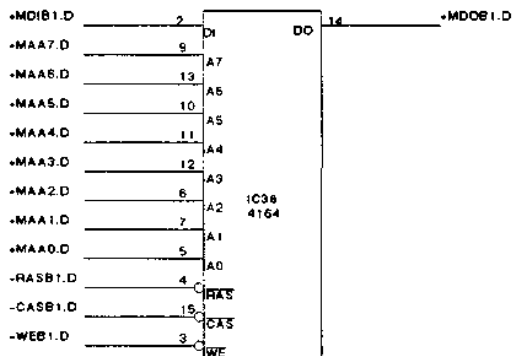
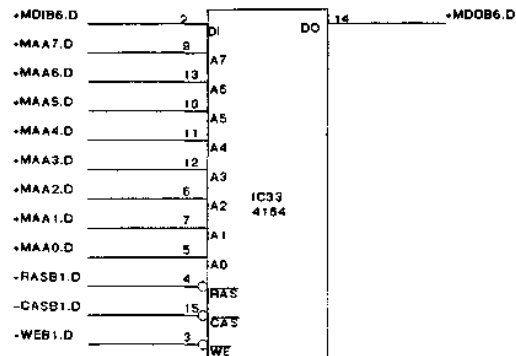
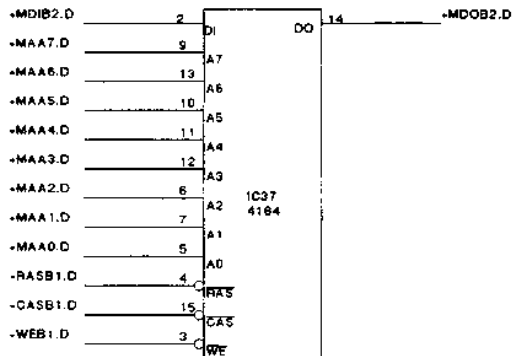
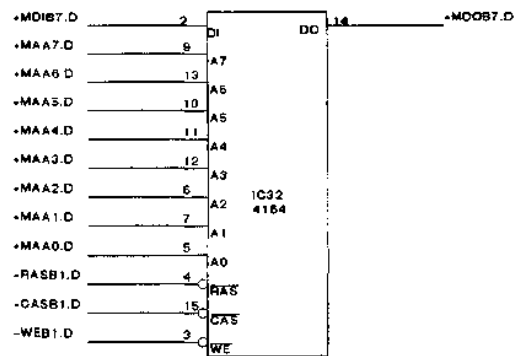
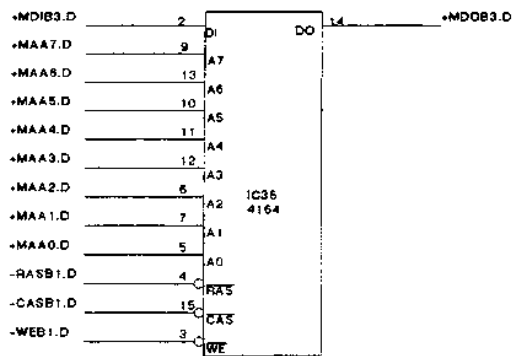


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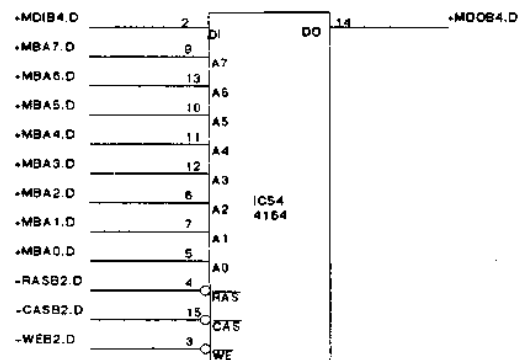
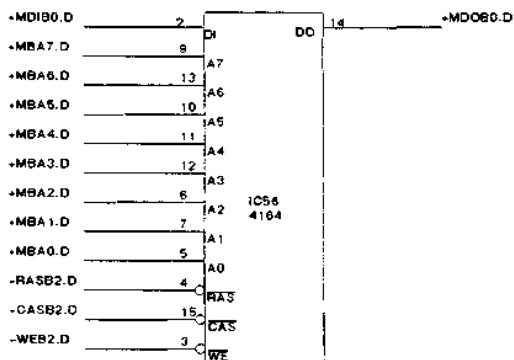
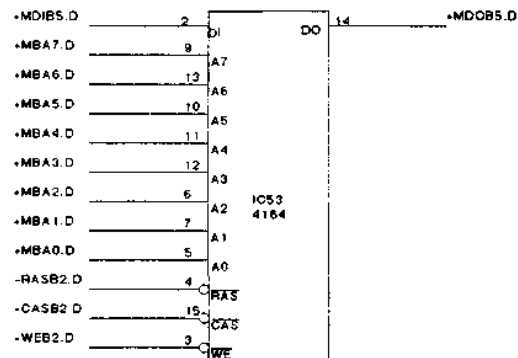
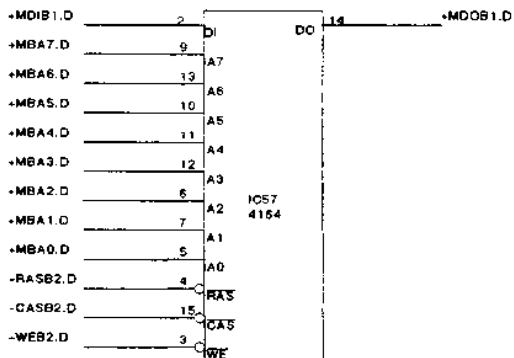
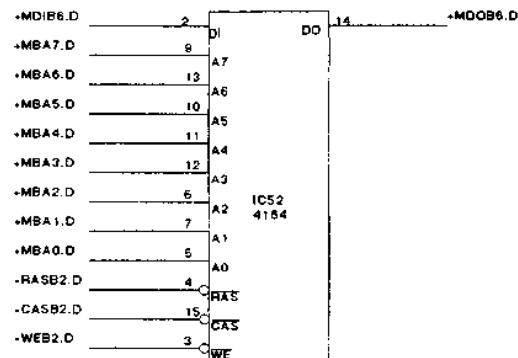
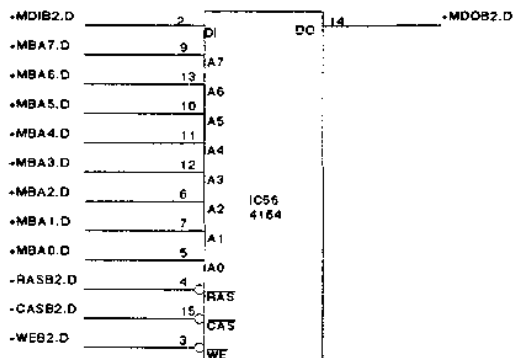
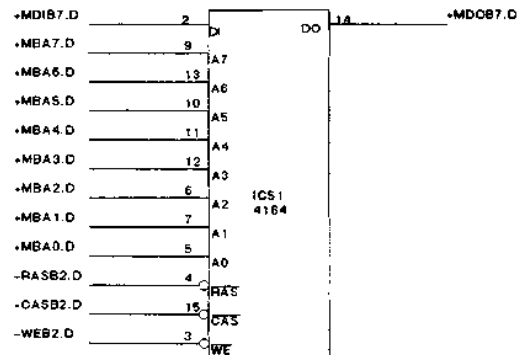
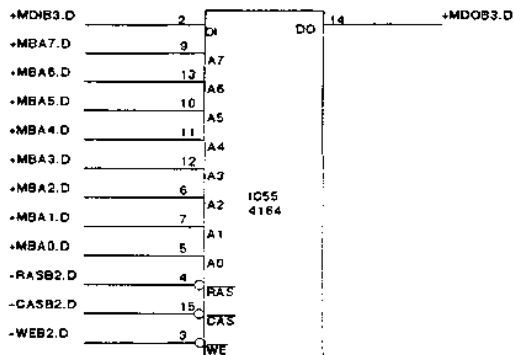


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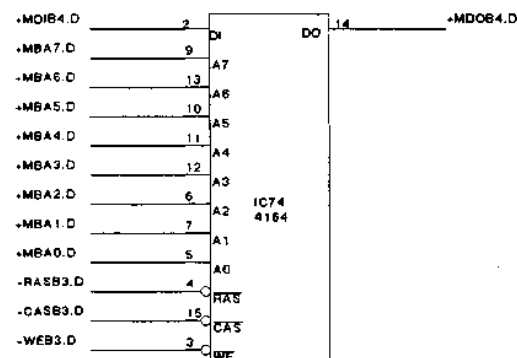
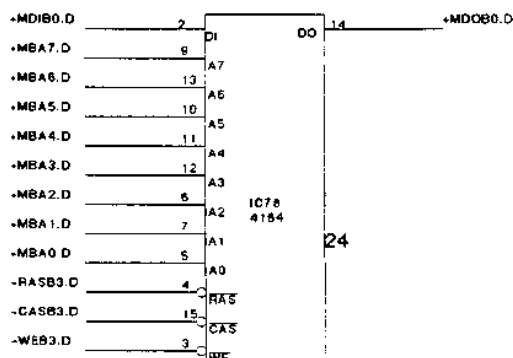
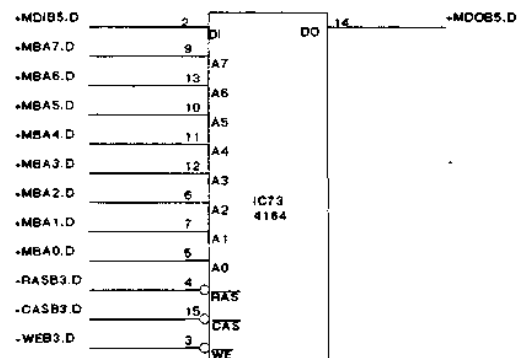
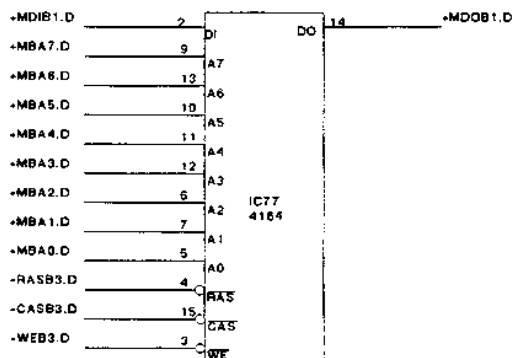
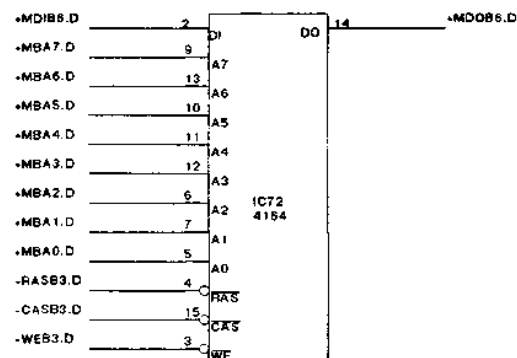
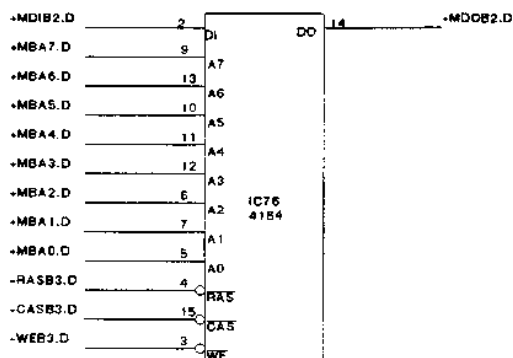
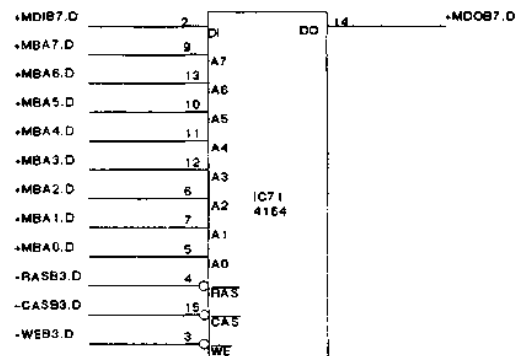
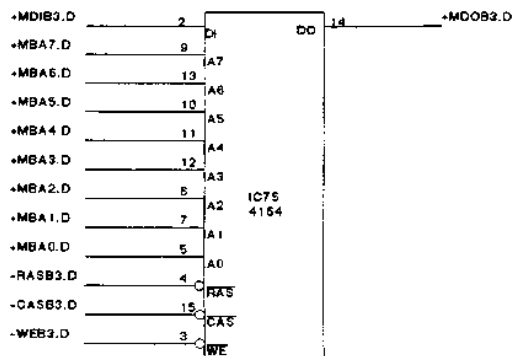


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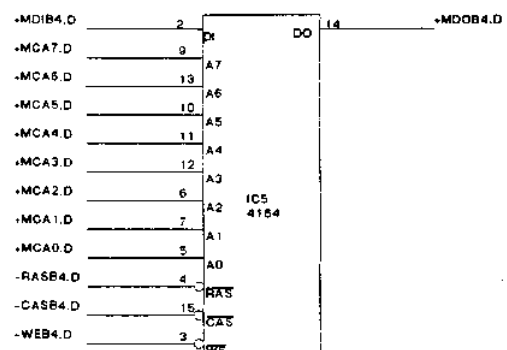
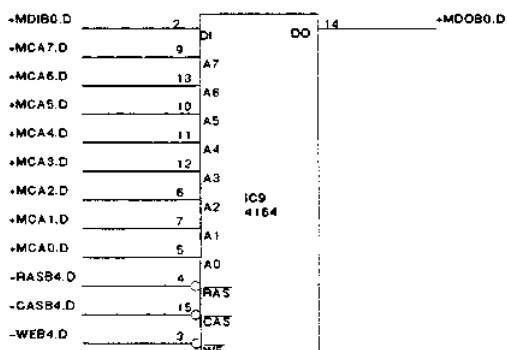
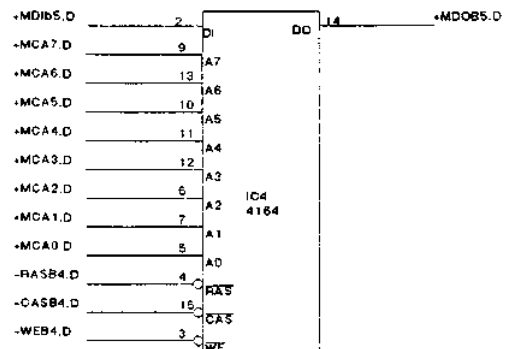
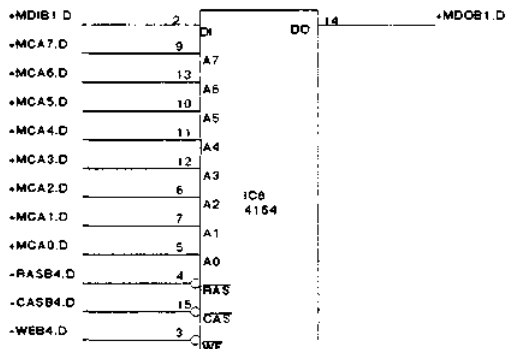
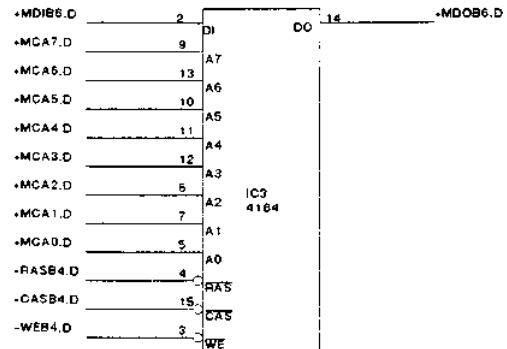
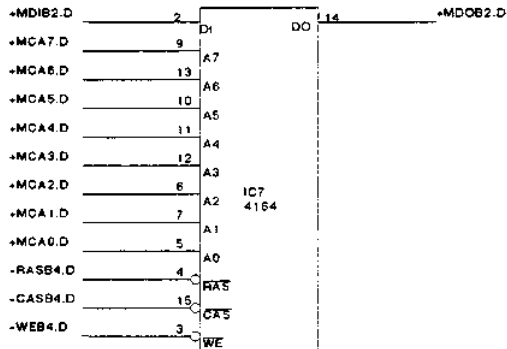
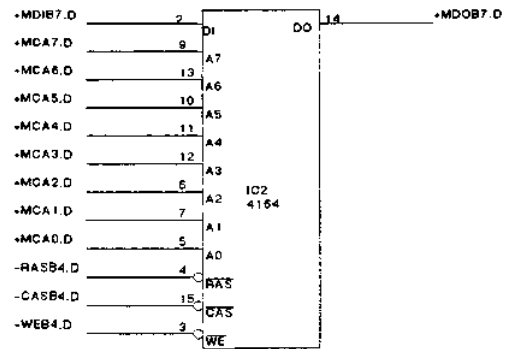
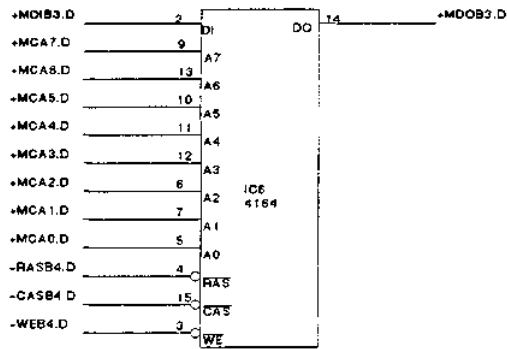


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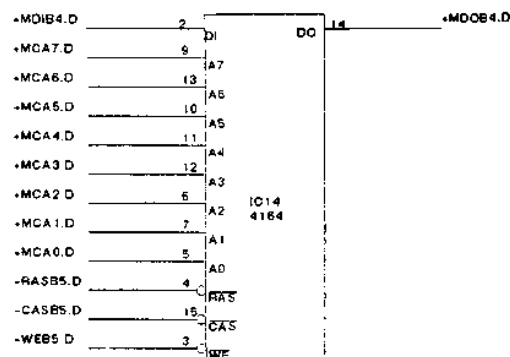
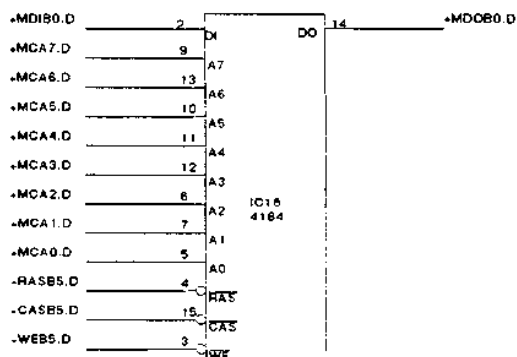
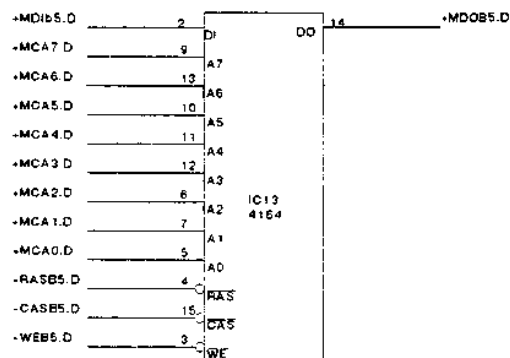
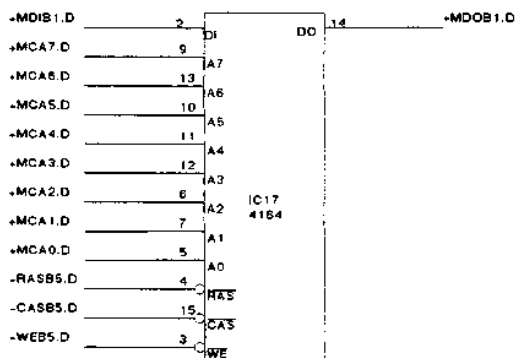
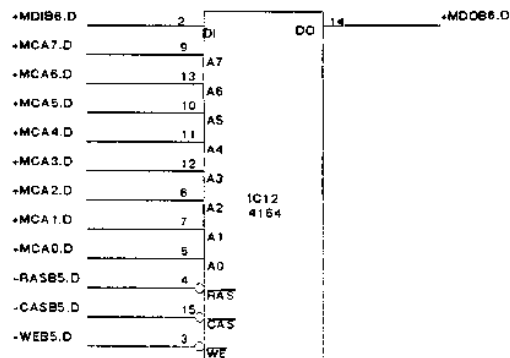
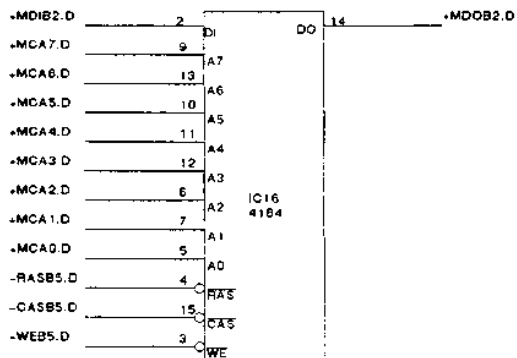
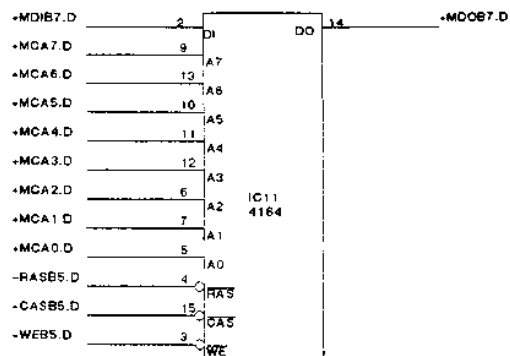
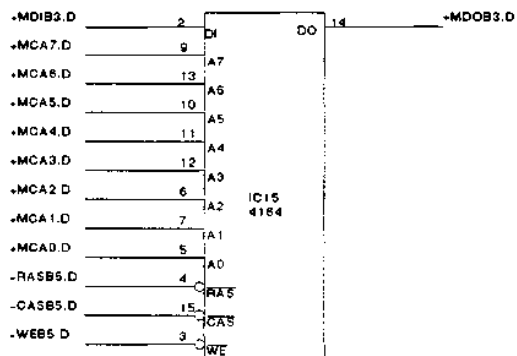


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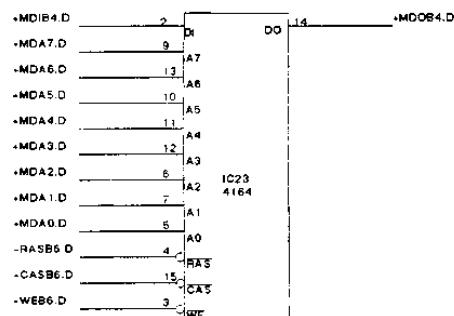
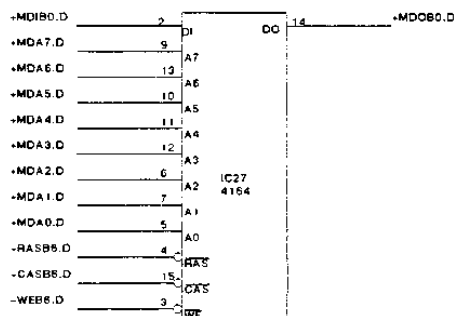
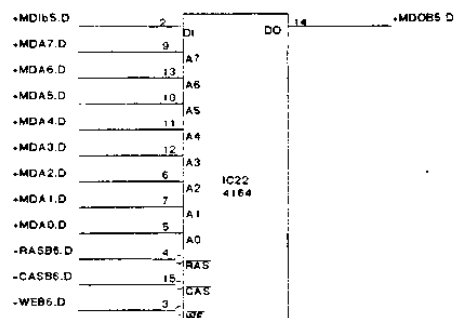
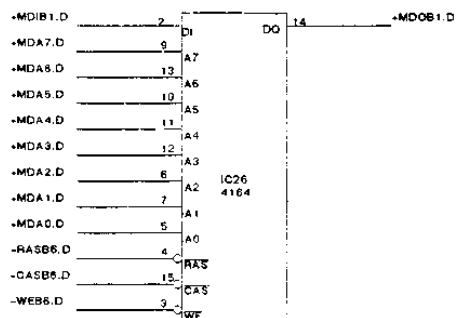
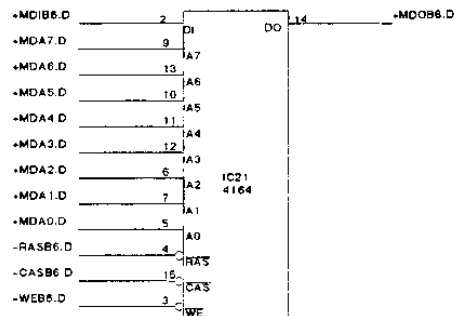
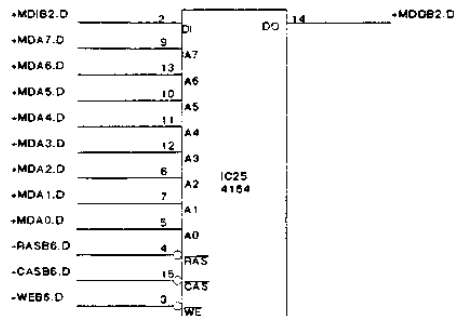
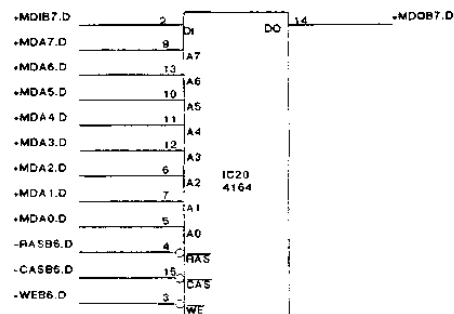
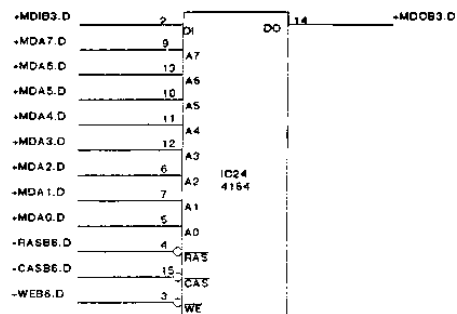


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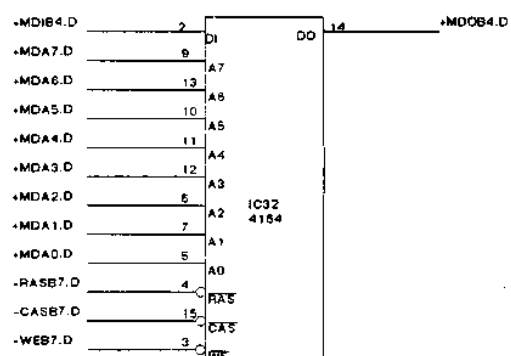
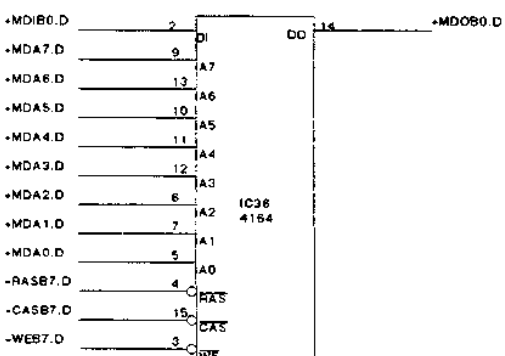
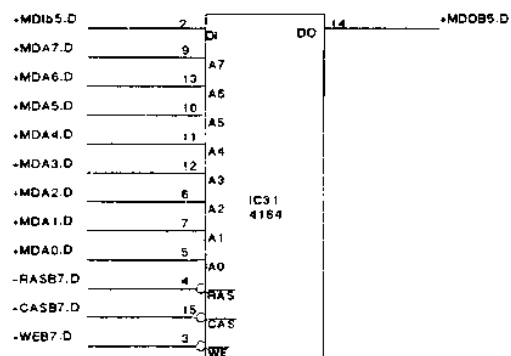
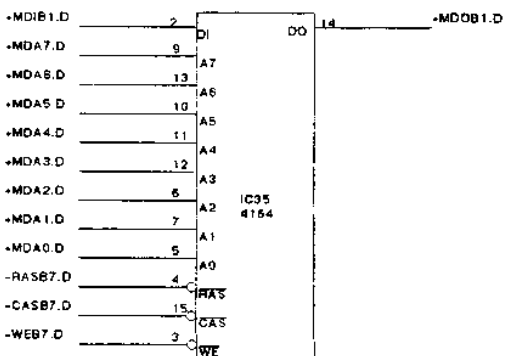
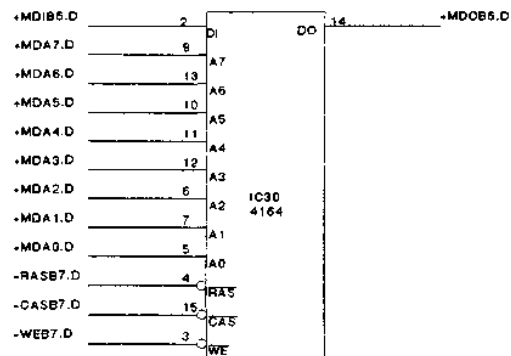
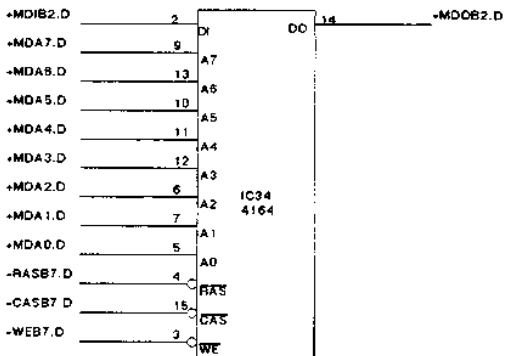
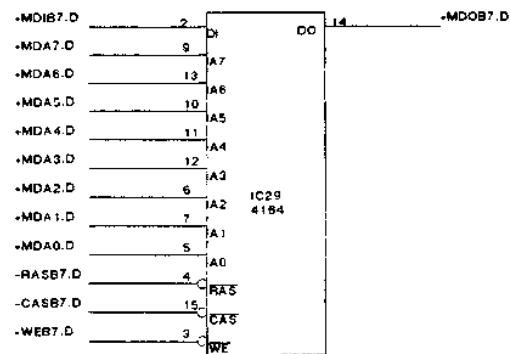
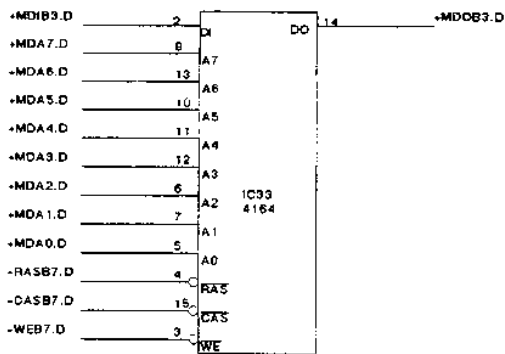


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