# Am2812 / Am2812A • Am2813 / Am2813A

## 32x8 and 32x9 First-In First-Out Memories

### Distinctive Characteristics

- Completely independent read and write operations
- "Half-full" flag
- Am2812 has serial or parallel input and output
- Data rates up to 1 MHz

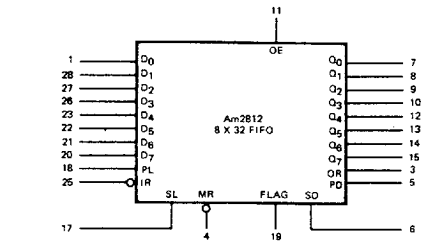
### FUNCTIONAL DESCRIPTION

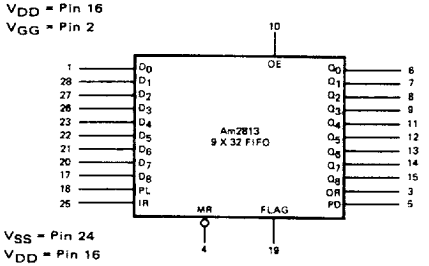
The Am2812 and Am2813 are 32 word by 8-bit and 9-bit first-in first-out memories, respectively. Both devices have completely independent read and write controls and have three-state outputs controlled by an output enable pin (OE). Data on the data inputs ($D_i$) are written into the memory by a pulse on load (PL). The data word automatically ripples through the memory until it reaches the output or another data word. Data is read from the memory by applying a shift out pulse on PD. This dumps the word on the outputs ($Q_i$) and the next word in the buffer moves to the output. An output ready signal (OR) indicates that data is available at the output and also provides a memory empty signal. An input ready (IR) signal indicates that the device is ready to accept data and also provides a memory full signal. Both the Am2812 and Am2813 have master reset inputs which clear all data from the device (reset to all LOWs), and a FLAG signal which goes HIGH when the memory contains more than 15 words.

The Am2812 can perform input and output data transfer on a bit-serial basis as well as on 8-bit parallel words. The input buffer is in reality an 8-bit shift register which can be loaded in parallel by the PL command or can be loaded serially through the $D_0$ input by using the SL clock. When 8 bits have been shifted into the input buffer serially, the 8-bit word automatically moves in parallel through the memory. The output includes a built-in parallel-to-serial converter, so that data can be shifted out of the $Q_7$ output by using the SD clock. After 8 clock pulses a new 8-bit word appears at the outputs.

The timing and function of the four control signals, PL, IR, PD, and OR, are designed so that two FIFOs can be placed end to end, with OR of the first driving PL of the second and IR of the second driving PD of the first. With this simple interconnection, strings of FIFOs can control each other reliably to make a FIFO array any number of words deep.

### LOGIC SYMBOLS

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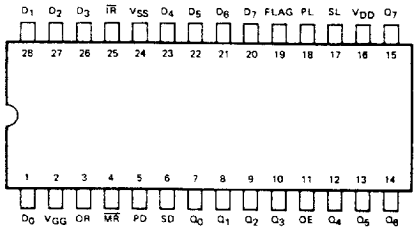
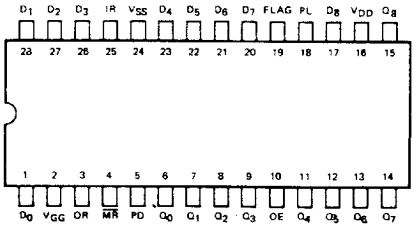
### CONNECTION DIAGRAMS
Top Views

Am2812




Am2813




Note: Pin 1 is marked for orientation.

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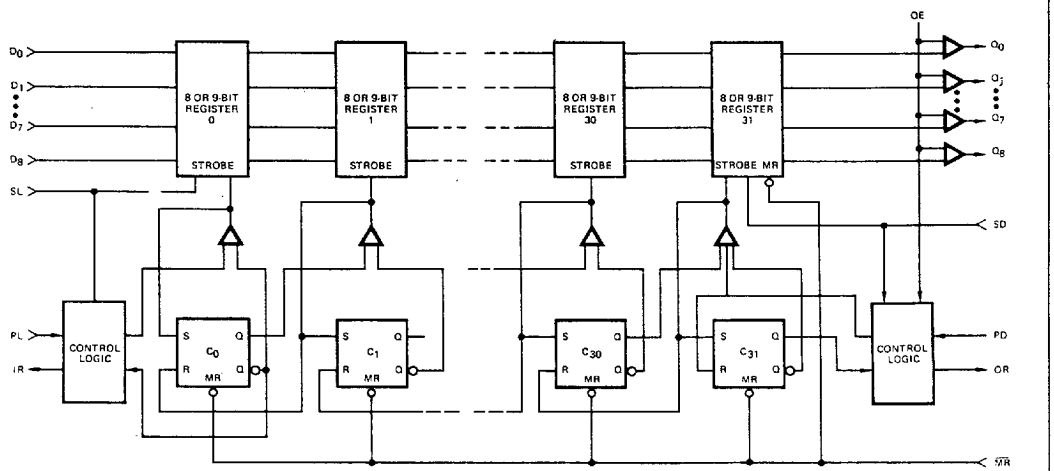
### ORDERING INFORMATION

| Package Type | Frequency | Temperature Range | Am2812 Order Number | Am2813 Order Number |
|---|---|---|---|---|
| Hermetic DIP | 500KHz | 0°C to +70°C | AM2812DC | AM2813DC |
| Hermetic DIP | 500KHz | −55°C to +85°C | AM2812DL | AM2813DL |
| Hermetic DIP | 1MHz | 0°C to +70°C | AM2812ADC | AM2813ADC |
| Hermetic DIP | 1MHz | −55°C to +85°C | AM2812ADL | AM2813ADL |
| Hermetic DIP | 500KHz | −55°C to +125°C | – | AM2813DM |
| Hermetic DIP | 1MHz | −55°C to +125°C | – | AM2813ADM |

## LOGIC BLOCK DIAGRAM




### DESCRIPTION OF THE Am2812 and Am2813 FIFO OPERATION

The Am2812 and Am2813 FIFOs consist internally of 32 data registers and one 32-bit control register, as shown in the logic block diagram. A "1" in a bit of the control register indicates that a data word is stored in the corresponding data register. A "0" in a bit of the control register indicates that the corresponding data register does not contain valid data. The control register directs the movement of data through the data registers. Whenever the $n^{th}$ bit of the control register contains a "1" and the (n+1)th bit contains a "0", then a strobe is generated causing the (n+1)th data register to read the contents of the $n^{th}$ data register, simultaneously setting the (n+1)th control register bit and clearing the $n^{th}$ control register bit, so that the control flag moves with the data. In this fashion data in the data register moves down the stack of data registers toward the output as long as there are "empty" locations ahead of it. The fall through operation stops when the data reaches a register n with a "1" in the (n+1)th control register bit, or the end of the register.

Data is initially loaded from the data inputs by applying a LOW-to-HIGH transition on the parallel load (PL) input. A "1" is placed in the first control register bit simultaneously. The first control register bit is returned buffered, to the input ready (IR) output, and this pin goes inactive indicating that data has been entered into the first data register and the input is now "busy", unable to accept more data. When PL next goes LOW, the fall-through process begins (assuming that at least the second location is empty). The data in the first register is copied into the second, and the first control register bit is cleared. This causes IR to go active, indicating the inputs are available for another data word.

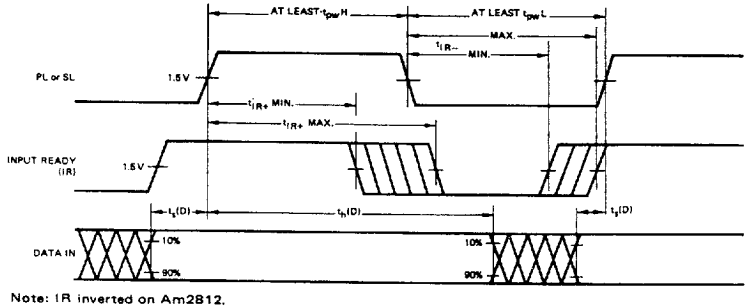
The data falling through the register stacks up at the output end. At the output the last control register bit is buffered and brought out as Output Ready (OR). A HIGH on OR indicates there is a "1" in the last control register bit and therefore there is valid data on the data outputs. A parallel dump command is used to shift the data word out of the FIFO. A LOW-to-HIGH transition on PD clears the last register bit, causing OR to go LOW, indicating that the data on the outputs may no longer be valid. When PD goes LOW, the "0" which is now present at the last control register bit allows the data in the next to the last register to move into the last register position and on to the outputs. The "0" in the control register then "bubbles" back toward the input as the data shifts toward the output.

If the memory is emptied by reading out all the data, then when the last word is being read out and PD goes HIGH, OR will go LOW as before, but when PD next goes LOW, there is no data to move into the last location, so OR remains LOW until more data arrives at the output. Similarly, when the memory is full data written into the first location will not shift into the second when PL goes LOW, and IR will remain inactive instead of returning to an active state.

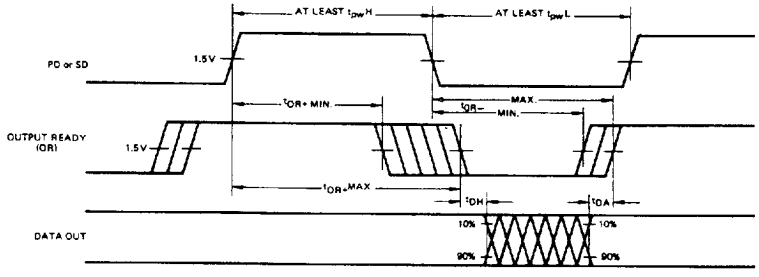
The pairs of input and output control signals are designed so that the PD input of one FIFO can be driven by the IR output of another, and the OR output of the first FIFO can drive the PL input of the second, allowing simple expansion of the FIFO to any depth. Wider buffers are formed by allowing parallel rows of FIFOs to operate together, as shown in the application on the last page.

Because the input ready signal is active LOW on the Am2812 a peculiarity occurs when several devices are placed end-to-end. When the second unit of two Am2812's fills up, the data out of the first is not dumped immediately. That is, no shift out command occurs, so that the data last written into the second device remains on the output of the first until an empty location bubbles up from the output. The net effect is that n Am2812s connected end-to-end store 31n+1 words (instead of 32n). The Am2813 stores 32n words in this configuration, because IR is active HIGH and does dump the last word written into the second device.

## TIMING DIAGRAM




Note: IR inverted on Am2812.

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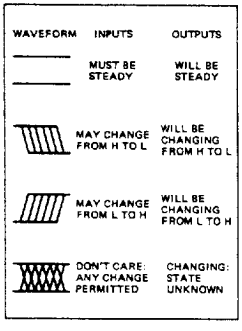
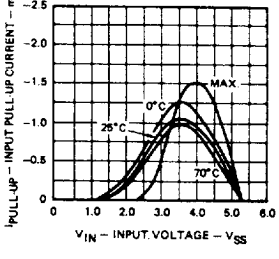
### USER NOTES

1. When the memory is empty the last word read will remain on the outputs until the master reset is strobed or a new data word falls through to the output. However, OR will remain LOW, indicating data at the output is not valid.
2. When the output data changes as a result of a pulse on PD, the OR signal always goes LOW before there is any change in output data and always stays LOW until after the new data has appeared on the outputs, so anytime OR is HIGH, there is good, stable data on the outputs.
3. If PD is held HIGH while the memory is empty and a word is written into the input, then that word will fall through the memory to the output. OR will go HIGH for one internal cycle (at least $t_{OR+}$) and then will go back LOW again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until PD has been brought LOW.
4. When the master reset is brought LOW, the control register and the outputs are cleared. $\overline{IR}$ goes HIGH and OR goes LOW. If PL is HIGH when the master reset goes HIGH then the data on the inputs will be written into the memory and $\overline{IR}$ will return to the HIGH state until PL is brought LOW. If PL is LOW when the master reset is ended, then $\overline{IR}$ will go LOW but the data on the inputs will not enter the memory until PL goes HIGH.
5. The output enable pin inhibits dump commands while it is LOW and forces the Q outputs to a high impedance state.
6. The serial load and dump lines should not be used for interconnecting two FIFOs. Use the parallel interconnection instead.
7. If less than eight bits have been shifted in using the serial load command, a parallel load pulse will destroy the data in the partially filled input register.

### KEY TO TIMING DIAGRAM




### Pull-up Characteristic Input Current Versus Input Voltage

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## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +85°C |
| $V_{DD}$ Supply Voltage | $V_{SS}$ −7V to $V_{SS}$ +0.3V |
| $V_{GG}$ Supply Voltage | $V_{SS}$ −20V to $V_{SS}$ +0.3V |
| DC Input Voltage | $V_{SS}$ −10V to $V_{SS}$ +0.3V |

## OPERATING RANGE

| Part Number | Ambient Temperature | $V_{SS}$ | $V_{DD}$ | $V_{GG}$ |
|---|---|---|---|---|
| Am2812DC, Am2812ADC | 0°C to +70°C | 5.0V ±5% | 0V | −12V ±5% |
| Am2813DC, Am2813ADC | | | | |
| Am2812DL, Am2812ADL | −55°C to +85°C | 5.0V ±5% | 0V | −12 ±5% |
| Am2813DL, Am2813ADL | | | | |
| Am2813DM, Am2813ADM | −55°C to +125°C | 5.0V ±5% | 0V | −12V ±5% |

## ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

| Parameters | Description | Test Conditions | | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = .300mA | | $V_{SS}$ −1.0 | | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 1.6mA | | | | 0.4 | V |
| $V_{IH}$ | Input HIGH Level | | | $V_{SS}$ −1.0 | | | V |
| $V_{IL}$ | Input LOW Level | | | | | 0.8 | V |
| $I_{IL}$ | Input Leakage Current | $V_{IN}$ = 0V (Note 2) | | | | 1.0 | µA |
| $I_{IH}$ (Note 2) | Input HIGH Current | $V_{IN}$ = $V_{SS}$ −1.0V (Note 2) | | 250 | | | µA |
| $V_{PUP}$ | Input Pull-up Initiation Voltage | (Note 2) | $V_{SS}$ = MIN. | | | 2.0 | V |
| | | | $V_{SS}$ = MAX. | | | 2.2 | V |
| $V_{BAR}$ | Voltage at Peak Input Current | (Note 2) | | | | $V_{SS}$ −1.5 | V |
| $I_{BAR}$ | Maximum Input Current | (Note 2) | | | | 1.6 | mA |
| $I_{GG}$ | $V_{GG}$ Current (Note 5) | $T_A$ = 0°C to +70°C | | | 14 | 22 | mA |
| | | $T_A$ = −55°C to +85°C | | | | 27 | |
| $I_{DD}$ | $V_{DD}$ Current | $T_A$ = 0°C to +70°C | | | 30 | 45 | mA |
| | | $T_A$ = −55°C to +85°C | | | | 55 | |

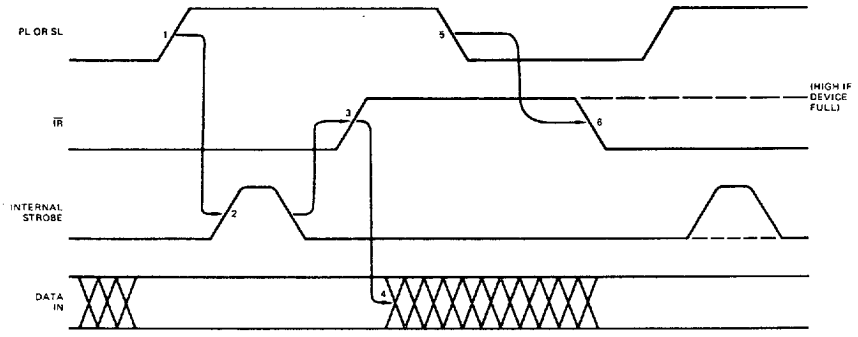
Notes: 1. Typical limits are at $V_{SS}$ = 5.0V, $V_{GG}$ = −12.0V, $T_A$ = 25°C
2. Pull up circuit on Am2813 only. See graph of input V-I characteristics.
3. Am2813ADM and Am2813ADM: $I_{GG}$ is guaranteed for $T_A$ = −55°C to +125°C

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Conditions/Note | Test Conditions | Am2812/Am2813 Min. | Typ. | Max. | Am2812A/Am2813A Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| $f_p$ | Maximum Parallel Load or Dump Frequency | | 0.5 | | | 1.0 | | | MHz |
| $t_{IR+}$ | Delay, PL or SL HIGH to IR In-Active | | 100 | 300 | 1100 | 80 | 300 | 450 | ns |
| $t_{IR-}$ | Delay, PL or SL LOW to IR Active | | 100 | 250 | 800 | 80 | 250 | 400 | ns |
| $t_{pw}H(P)$ | Minimum PL or PD HIGH Time | | 100 | | 100 | 80 | | | ns |
| $t_{pw}L(P)$ | Minimum PL or PD LOW Time | | 100 | | 100 | 80 | | | ns |
| $t_{pw}H(S)$ | Minimum SL or SD HIGH Time | Am2812 only | 350 | | 350 | 300 | | | ns |
| $t_{pw}H(P)$ | Minimum PL or PD HIGH Time | Am2813ADM Only | | | | 200 | | | ns |
| $t_{pw}L(P)$ | Minimum PL or PD LOW Time | Am2813ADM Only | | | | 200 | | | ns |
| $t_{pw}L(S)$ | Minimum SL or SD LOW Time | Am2812 only | 350 | | 350 | 300 | | | ns |
| $t_h(D)$ | Data Hold Time | | | 190 | 300 | | 170 | 250 | ns |
| $t_s(D)$ | Data Set-Up Time | to PL | | | 0 | | | 0 | ns |
| | | to SL | | | 100 | | | 90 | |
| $t_{OR+}$ | Delay, PD or SD HIGH to OR LOW | OE HIGH | 100 | 450 | 1100 | 100 | 350 | 520 | ns |
| $t_{OR-}$ | Delay, PD or SD LOW to OR HIGH | OE HIGH | 100 | 400 | 850 | 100 | 300 | 470 | ns |
| $t_{PT}$ | Ripple through Time | FIFO Empty | | | 10 | | | 8 | µs |
| $t_{DH}$ | Delay, OR LOW to Data Out Changing | PD = LOW | 50 | 200 | | 50 | 200 | | ns |
| $t_{DA}$ | Delay, Data Out to OR HIGH | PD = HIGH | 0 | 100 | | 0 | 100 | | ns |
| $t_{MRW}$ | Minimum Reset Pulse Width | | | | 600 | | | 500 | ns |
| $t_{DO}$ | Delay, OE LOW to Output OFF | | | | 600 | | | 500 | ns |
| $t_{EO}$ | Delay, OE HIGH to Output Active | | | | 600 | | | 500 | ns |
| $t_{DF}$ | Delay from PL or SL HIGH to Flag HIGH or PD or SD HIGH to Flag LOW | | | 0.5 | 1.0 | | 0.5 | 1.0 | µs |
| CI | Input Capacitance | | | | 7 | | | 7 | pF |

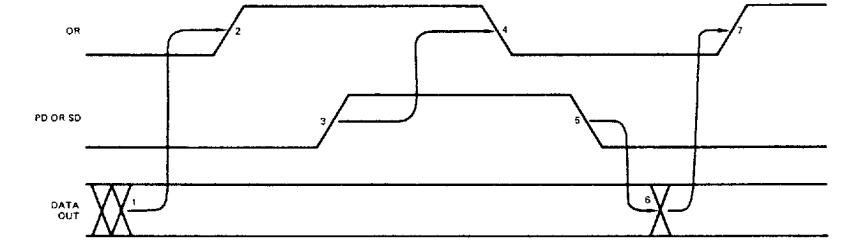
Notes: 3. IR is active HIGH on Am2813 and active LOW on Am2812.
4. Minimum and maximum delays generally occur at opposite temperature extremes. Devices at approximately the same temperature will have compatible switching characteristics and will drive each other.

## Am2812 TIMING DIAGRAM




### Am2812 INPUT TIMING

When data is steady PL is brought HIGH (1) causing internal data strobe to be generated (2). When data has been loaded, $\overline{IR}$ goes HIGH (3) and data may be changed (4). $\overline{IR}$ remains HIGH until PL is brought LOW (5); then $\overline{IR}$ goes LOW (6) indicating new data may be entered.




### Am2812 OUTPUT TIMING

When data out is steady (1), OR goes HIGH (2). When PD goes HIGH (3), OR goes LOW (4). When PD goes LOW again (5), the output data changes (6) and OR returns HIGH (7).

The input and output timing diagrams above illustrate the sequence of control on the Am2812. Note that PL matches OR and $\overline{IR}$ matches PD in time, as though the signals were driving each other. The Am2813 pattern is similiar, but IR is active HIGH instead of active LOW (shown in timing diagram on next page).

### FLAG OUTPUT

A flag output is available on the Am2812 and Am2813 to indicate whether the FIFO is more or less than half full. The flag signal is generated by summing the "1s" in the control flip-flops, and therefore is not affected by the movement of data through the register. The flag signal goes HIGH when the 13th, 14th, 15th, or 16th word is loaded into the FIFO. It will remain HIGH until there are less than 15+1/−2 words in the memory. It is always HIGH if there are more than 16 words in the FIFO.

### RESET

An over-riding master reset ($\overline{MR}$) is used to clear all control register bits and set all the outputs LOW.

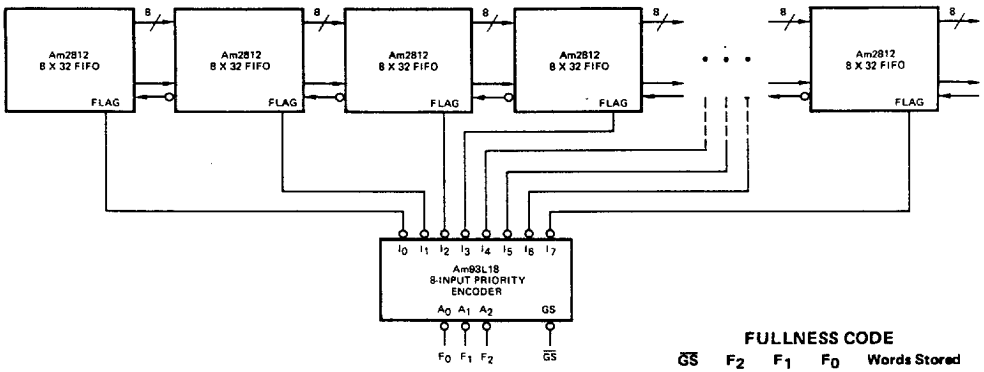
### SERIAL INPUT AND OUTPUT (Am2812 ONLY)

The Am2812 also has the ability to read or write serial bit streams, rather than 8-bit words. The device then works like a 256 by 1-bit FIFO. A serial data stream can be loaded into the device by using the serial load input and applying data to $D_0$ input. Inputs $D_1$—$D_7$ must be grounded. The SL signal operates just like the PL input, causing IR to go HIGH and LOW as the bits are entered. The data is simply shifted across the 8-bit input register until 8 bits have been entered; the 8 bits then fall through the register as though they had been loaded in parallel. Following the 8th SL pulse, IR will remain inactive if the FIFO is full.

A corresponding operation occurs on the output, with clock pulses on SD causing successive bits of data to appear on the $O_7$ output. OR moves HIGH and LOW with SD exactly as it does with PD. When 8 bits have been shifted out, the next word appears at the output. If a PD command is applied after the 8 bits on the outputs have been partially shifted out, the remainder of the word is dumped and a new 8-bit word is brought to the output. OR will stay LOW if the FIFO is empty.

When the serial input or output clock is used, the corresponding parallel control line should be grounded and when the PD or PL controls are used the corresponding serial clocks should be grounded.

## APPLICATIONS



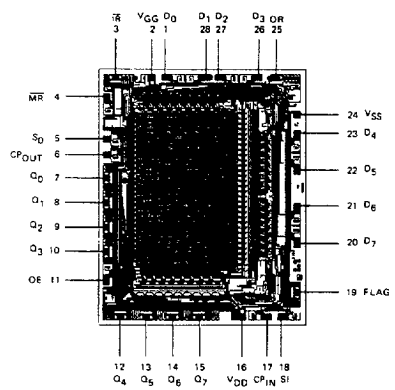

**FULLNESS CODE**

| $\overline{GS}$ | $F_2$ | $F_1$ | $F_0$ | Words Stored |
|---|---|---|---|---|
| L | L | L | L | 0 – 15 |
| L | L | L | H | 13 – 47 |
| L | L | H | L | 45 – 78 |
| L | L | H | H | 76 – 109 |
| L | H | L | L | 107 – 140 |
| L | H | L | H | 138 – 171 |
| L | H | H | L | 169 – 202 |
| L | H | H | H | 200 – 233 |
| H | H | H | H | 231 – 249 |

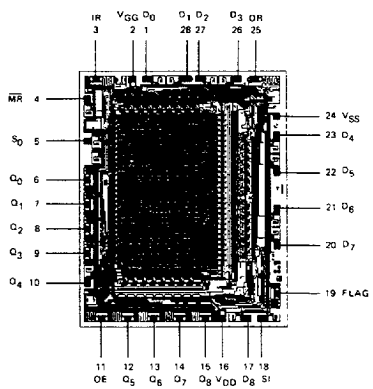
The Fullness Flags from Am2812 or Am2813 FIFOs can be encoded by an Am93L18 8-input priority encoder. The output code $F_0$-$F_2$ indicates the weight of the highest priority input which is LOW. GS is group signal; it is HIGH if all the inputs are HIGH.

### Metallization and Pad Layouts

**Am2812**




**Am2813**




DIE SIZE 0.128" X 0.168"